Design For High Performance Low Power And Reliable 3d Integrated Circuits

As recognized, adventure as without difficulty as experience virtually lesson, amusement, as with ease as conformity can be gotten by just checking out a ebook **Design For High Performance Low Power And Reliable 3d Integrated Circuits** next it is not directly done, you could tolerate even more in this area this life, roughly speaking the world.

We present you this proper as well as easy exaggeration to acquire those all. We provide Design For High Performance Low Power And Reliable 3d Integrated Circuits and numerous books collections from fictions to scientific research in any way. along with them is this Design For High Performance Low Power And Reliable 3d Integrated Circuits that can be your partner.

An ASIC Low Power Primer - Rakesh Chadha 2012-12-05
This book provides an invaluable primer on the techniques utilized in the design of low power digital semiconductor devices. Readers will benefit from the hands-on approach which starts form the ground-up, explaining with basic examples what power is, how it is measured and how it impacts on the design process of application-specific integrated circuits (ASICs). The authors use both the Unified Power Format (UPF) and Common Power Format (CPF) to describe in detail the power intent for an ASIC and then guide readers through a variety of architectural and implementation techniques that will help meet the power intent. From analyzing system power consumption, to techniques that can be employed in a low power design, to a detailed description of two alternate standards for capturing the power directives at various phases of the design, this book is filled with information that will give ASIC designers a competitive edge in low-power design.
Structured Electronic Design - Arie van Staveren 2006-04-18
Analog design still has, unfortunately, a flavor of art. Art can be beautiful. However, art in itself is difficult to teach to students and difficult to transfer from experienced analog designers to new trainee designers in companies. Structured Electronic Design: High-Performance Harmonic Oscillators and Bandgap References aims to systemize analog design. The use of orthogonalization of the design of the fundamental quality aspects (noise, distortion, and bandwidth) and hierarchy in the subsequent design steps, enables designers to achieve high-performance designs, in a relatively short time. As a result of the systematic design procedure, the effect of design decisions on the circuit performance is made clear. Additionally, the use of resources for reaching a specified performance is tracked. This book, therefore, describes the structured electronic design of high-performance harmonic oscillators and bandgap references. The structured design of harmonic oscillators includes the maximization of the carrier-to- noise ratio by means of tapping, i.e. an impedance adaption method for noise matching. The bandgap reference, a popular implementation of a voltage reference, is studied via the unusual concept of the linear combination of base-emitter voltages. The presented method leads to the design of high-

performance references in CMOS and Bipolar technology. Using this concept, on a high level of abstraction the quality with respect to, for instance, noise and power-supply rejection can be identified. In this book, it is shown with several design examples that this method provides an excellent starting point for the design of high-performance bandgap references. Auxiliary to the harmonic-oscillator and bandgap reference design are the negative- feedback amplifiers. In this book the systematic design of the dynamic behavior is emphasized. By means of the identification of the dominant poles, it is possible to give an upper limit of the attainable bandwidth, even before the real frequency compensation is accomplished. Structured Electronic Design: High-Performance Harmonic Oscillators and Bandgap References is a valuable book for researchers and designers, as well as students in the field of analog design. It helps both the experienced and trainee designer to come to grips with the design of analog circuits. The presented method is illustrated by several well-described design examples.

Advances in VLSI, Communication, and Signal Processing - Amit Dhawan 2022-10-04

This book comprises select peer-reviewed proceedings of the International Conference on VLSI, Communication and Signal processing (VCAS 2021). The contents focus on the latest research in different domains of electronics and communication engineering, in particular microelectronics and VLSI design, communication systems and networks, and signal and image processing. The book discusses the emerging applications of novel tools and techniques in image, video, and multimedia signal processing. This book will be useful to students, researchers, and professionals working in electronics and communication.

Structured Electronic Design of High-performance Low-voltage Low-power References - Arie van Staveren 1997

Advances in Signal Processing and Communication - Banmali S. Rawat 2018-11-19

This book is a collection of selected peer-reviewed papers presented at the International Conference on Signal Processing and Communication (ICSC 2018). It covers current research and developments in the fields of communications, signal processing, VLSI circuits and systems, and embedded systems. The book offers in-depth discussions and analyses of latest problems across different sub-fields of signal processing and communications. The contents of this book will prove to be useful for students, researchers, and professionals working in electronics and electrical engineering, as well as other allied fields.

Computational Science and Its Applications - ICCSA 2006 - Marina Gavrilova 2006-05-05

The five-volume set LNCS 3980-3984 constitutes the refereed proceedings of the International Conference on Computational Science and Its Applications, ICCSA 2006. The volumes present a total of 664 papers organized according to the five major conference themes: computational methods, algorithms and applications high performance technical computing and networks advanced and emerging applications geometric modelling, graphics and visualization information systems and information technologies. This is Part V.

Low-Power NoC for High-Performance SoC Design - Hoi-Jun Yoo 2018-10-08

Chip Design and Implementation from a Practical Viewpoint Focusing on chip implementation, Low-Power NoC for High-Performance SoC Design provides practical knowledge and real examples of how to use network on chip (NoC) in the design of system on chip (SoC). It discusses many architectural and theoretical studies on NoCs, including design methodology, topology exploration, quality-of-service guarantee, low-power design, and implementation trials. The Steps to Implement NoC The book covers the full spectrum of the subject, from theory to actual chip design using NoC. Employing the Unified Modeling

Language (UML) throughout, it presents complicated concepts, such as models of computation and communication–computation partitioning, in a manner accessible to laypeople. The authors provide guidelines on how to simplify complex networking theory to design a working chip. In addition, they explore the novel NoC techniques and implementations of the Basic On-Chip Network (BONE) project. Examples of real-time decisions, circuit-level design, systems, and chips give the material a real-world context. Low-Power NoC and Its Application to SoC Design Emphasizing the application of NoC to SoC design, this book shows how to build the complicated interconnections on SoC while keeping a low power consumption.

Design of High Performance, Low Power Latches and Flip-flops - Shridhar Mubaraq Mishra 1999

High Performance Analog and Power Management Circuit Design Techniques for Modern SoCs - Annajirao Garimella 2016-01-08

This book illustrates some of the recent state-of-the-art advances in Analog and Power Management circuit design. Coverage includes design of advanced low-power/low-voltage analog circuits, small-signal and pole-zero analysis of multi-stage amplifiers, state-of-the-art frequency compensation topologies, and advanced power management circuits and control techniques. Readers will benefit from detailed small-signal techniques for complex multi-stage amplifiers and low drop-out voltage regulators (LDOs), a ubiquitous power management circuit. The authors provide tutorial treatment of frequency compensation techniques while illustrating some of the state-of-the-art techniques. The authors also discuss in detail the challenges in the design of modern power management circuits, including low dropout voltage regulators, switched-capacitor DC-to-DC converters and inductor-based DC-DC converters.

High Performance Architecture and Grid Computing - Archana Mantri 2011-07-05

This book constitutes the refereeds proceedings of the International Conference on High Performance Architecture and Grid Computing, HPAGC 2011, held in Chandigarh, India, in July 2011. The 87 revised full papers presented were carefully reviewed and selected from 240 submissions. The papers are organized in topical sections on grid and cloud computing; high performance architecture; information management and network security.

Low Power Design with High-Level Power Estimation and Power-Aware Synthesis - Sumit Ahuja 2011-10-22

This book presents novel research techniques, algorithms, methodologies and experimental results for high level power estimation and power aware high-level synthesis. Readers will learn to apply such techniques to enable design flows resulting in shorter time to market and successful low power ASIC/FPGA design.

VLSI-SoC: Design Trends - Andrea Calimera 2021-07-14

This book contains extended and revised versions of the best papers presented at the 28th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2020, held in Salt Lake City, UT, USA, in October 2020.* The 16 full papers included in this volume were carefully reviewed and selected from the 38 papers (out of 74 submissions) presented at the conference. The papers discuss the latest academic and industrial results and developments as well as future trends in the field of System-on-Chip (SoC) design, considering the challenges of nano-scale, state-of-the-art and emerging manufacturing technologies. In particular they address cutting-edge research fields like low-power design of RF, analog and mixed-signal circuits, EDA tools for the synthesis and verification of heterogenous SoCs, accelerators for cryptography and deep learning and on-chip Interconnection system, reliability and testing, and integration of 3D-ICs. *The conference was held virtually.

Current Sense Amplifiers for Embedded SRAM in High-Performance System-on-a-Chip Designs - Bernhard Wicht 2003-04-14
This book provides a systematic and comprehensive insight into current sensing techniques. In addition to describing theoretical and practical aspects of current sensing, the author derives practical design guidelines for achieving an optimal performance through a systematic analysis of different circuit principles. Voltage sense amplifiers are also considered, since they are used as a final comparator in a current sense amplifier. Innovative concepts, such as compensation of the bitline multiplexer and auto-power-down, are elucidated. Although the focus is on embedded static random access memory (SRAM), the material presented applies to any current-providing memory type, e.g. also to emerging memory technologies such as MRAM. The book will appeal to design engineers in industry and also to researchers wishing to learn about, and apply, current sensing techniques.
Design of High-Performance Microprocessor Circuits - Anantha Chandrakasan 2001
The authors present readers with a compelling, one-stop, advanced system perspective on the intrinsic issues of digital system design. This invaluable reference prepares readers to meet the emerging challenges of the device and circuit issues associated with deep submicron technology. It incorporates future trends with practical, contemporary methodologies.
High Performance Embedded Computing Handbook - David R. Martinez 2018-10-03
Over the past several decades, applications permeated by advances in digital signal processing have undergone unprecedented growth in capabilities. The editors and authors of High Performance Embedded Computing Handbook: A Systems Perspective have been significant contributors to this field, and the principles and techniques presented in the handbook are reinforced by examples drawn from their work. The chapters cover system components found in today’s HPEC systems by addressing design trade-offs, implementation options, and techniques of the trade, then solidifying the concepts with specific HPEC system examples. This approach provides a more valuable learning tool, Because readers learn about these subject areas through factual implementation cases drawn from the contributing authors’ own experiences. Discussions include: Key subsystems and components Computational characteristics of high performance embedded algorithms and applications Front-end real-time processor technologies such as analog-to-digital conversion, application-specific integrated circuits, field programmable gate arrays, and intellectual property–based design Programmable HPEC systems technology, including interconnection fabrics, parallel and distributed processing, performance metrics and software architecture, and automatic code parallelization and optimization Examples of complex HPEC systems representative of actual prototype developments Application examples, including radar, communications, electro-optical, and sonar applications The handbook is organized around a canonical framework that helps readers navigate through the chapters, and it concludes with a discussion of future trends in HPEC systems. The material is covered at a level suitable for practicing engineers and HPEC computational practitioners and is easily adaptable to their own implementation requirements.
Digital System Design - Use of Microcontroller - Shenouda Dawoud 2022-09-01
Embedded systems are today, widely deployed in just about every piece of machinery from toasters to spacecraft. Embedded system designers face many challenges. They are asked to produce increasingly complex systems using the latest technologies, but these technologies are changing faster than ever. They are asked to produce better quality designs with a shorter time-to-market. They are asked to implement increasingly complex functionality but more importantly to satisfy numerous other constraints. To achieve the current goals of design, the designer must be aware

with such design constraints and more importantly, the factors that have a direct effect on them.One of the challenges facing embedded system designers is the selection of the optimum processor for the application in hand; single-purpose, general-purpose or application specific. Microcontrollers are one member of the family of the application specific processors.The book concentrates on the use of microcontroller as the embedded system?s processor, and how to use it in many embedded system applications. The book covers both the hardware and software aspects needed to design using microcontroller.The book is ideal for undergraduate students and also the engineers that are working in the field of digital system design.Contents• Preface;• Process design metrics;• A systems approach to digital system design;• Introduction to microcontrollers and microprocessors;• Instructions and Instruction sets;• Machine language and assembly language;• System memory; Timers, counters and watchdog timer;• Interfacing to local devices / peripherals;• Analogue data and the analogue I/O subsystem;• Multiprocessor communications;• Serial Communications and Network-based interfaces.

Computational Science and Its Applications - ICCSA 2006 - Osvaldo Gervasi 2006-05-11

The five-volume set LNCS 3980-3984 constitutes the refereed proceedings of the International Conference on Computational Science and Its Applications, ICCSA 2006. The volumes present a total of 664 papers organized according to the five major conference themes: computational methods, algorithms and applications high performance technical computing and networks advanced and emerging applications geometric modelling, graphics and visualization information systems and information technologies. This is Part IV.

Low Power VLSI Design and Technology -

The VLSI Handbook - Wai-Kai Chen 2018-10-03

For the new millenium, Wai-Kai Chen introduced a monumental reference for the design, analysis, and prediction of VLSI circuits: The VLSI Handbook. Still a valuable tool for dealing with the most dynamic field in engineering, this second edition includes 13 sections comprising nearly 100 chapters focused on the key concepts, models, and equations. Written by a stellar international panel of expert contributors, this handbook is a reliable, comprehensive resource for real answers to practical problems. It emphasizes fundamental theory underlying professional applications and also reflects key areas of industrial and research focus. WHAT'S IN THE SECOND EDITION? Sections on... Low-power electronics and design VLSI signal processing Chapters on... CMOS fabrication Content-addressable memory Compound semiconductor RF circuits High-speed circuit design principles SiGe HBT technology Bipolar junction transistor amplifiers Performance modeling and analysis using SystemC Design languages, expanded from two chapters to twelve Testing of digital systems Structured for convenient navigation and loaded with practical solutions, The VLSI Handbook, Second Edition remains the first choice for answers to the problems and challenges faced daily in engineering practice.

Low-Power NoC for High-Performance SoC Design - Hoi-Jun Yoo 2018-10-08

Chip Design and Implementation from a Practical Viewpoint Focusing on chip implementation, Low-Power NoC for High-Performance SoC Design provides practical knowledge and real examples of how to use network on chip (NoC) in the design of system on chip (SoC). It discusses many architectural and theoretical studies on NoCs, including design methodology, topology exploration, quality-of-service guarantee, low-power design, and implementation trials. The Steps to Implement NoC The book covers the full spectrum of the subject, from theory to actual chip design using NoC. Employing the Unified Modeling Language (UML) throughout, it presents complicated concepts,

such as models of computation and communication–computation partitioning, in a manner accessible to laypeople. The authors provide guidelines on how to simplify complex networking theory to design a working chip. In addition, they explore the novel NoC techniques and implementations of the Basic On-Chip Network (BONE) project. Examples of real-time decisions, circuit-level design, systems, and chips give the material a real-world context. Low-Power NoC and Its Application to SoC Design Emphasizing the application of NoC to SoC design, this book shows how to build the complicated interconnections on SoC while keeping a low power consumption.

Modeling and Optimization of Parallel and Distributed Embedded Systems - Arslan Munir 2016-02-08

This book introduces the state-of-the-art in research in parallel and distributed embedded systems, which have been enabled by developments in silicon technology, micro-electro-mechanical systems (MEMS), wireless communications, computer networking, and digital electronics. These systems have diverse applications in domains including military and defense, medical, automotive, and unmanned autonomous vehicles. The emphasis of the book is on the modeling and optimization of emerging parallel and distributed embedded systems in relation to the three key design metrics of performance, power and dependability. Key features: Includes an embedded wireless sensor networks case study to help illustrate the modeling and optimization of distributed embedded systems. Provides an analysis of multi-core/many-core based embedded systems to explain the modeling and optimization of parallel embedded systems. Features an application metrics estimation model; Markov modeling for fault tolerance and analysis; and queueing theoretic modeling for performance evaluation. Discusses optimization approaches for distributed wireless sensor networks; high-performance and energy-efficient techniques at the architecture, middleware and software levels for parallel multicore-based embedded systems; and dynamic optimization methodologies. Highlights research challenges and future research directions. The book is primarily aimed at researchers in embedded systems; however, it will also serve as an invaluable reference to senior undergraduate and graduate students with an interest in embedded systems research.

CPU Design - Chandra Thimmannagari 2005-12-02

Presents information in a user-friendly, easy-access way so that the book can act as either a quick reference for more experienced engineers or as an introductory guide for new engineers and college graduates.

Synthesis of High Performance Low Power Cmos Circuit Design - Neelam Swami 2012-07

Latches and flip-flops used in low power sequential circuits are discussed in this book. A synthesis technique for power optimization in combinational logic circuits has been described. A flip flop has been proposed to reduce power consumption in CMOS circuits. A latch has been proposed which is evaluated from the standard ultra voltage latch for low power application. Simulation results show that the proposed latch has the lowest power consumption with no speed penalty. The significant power and area savings can be achieved by using proposed design.

Emerging Devices for Low-Power and High-Performance Nanosystems - Simon Deleonibus 2018-12-13

The history of information and communications technologies (ICT) has been paved by both evolutive paths and challenging alternatives, so-called emerging devices and architectures. Their introduction poses the issues of state variable definition, information processing, and process integration in 2D, above IC, and in 3D. This book reviews the capabilities of integrated nanosystems to match low power and high performance either by hybrid and heterogeneous CMOS in 2D/3D or by emerging devices for alternative sensing, actuating, data storage, and processing. The choice of future ICTs will need to take into account not only their energy efficiency but also their sustainability in the global

ecosystem.

Integrated Circuit and System Design: Power and Timing Modeling, Optimization and Simulation - José Monteiro 2010-02-18

Welcome to the proceedings of the 19th International Workshop on Power and TimingModeling,OptimizationandSimulation,PATMOS2009.Overthe years, PATMOShasevolvedintoanimportantEuropeanevent,whereresearchersfrom both industry and academia discuss and investigate the emerging challenges in future and contemporary applications, design methodologies, and tools required for the development of the upcoming generations of integrated circuits and s- tems. PATMOS 2009 was organized by TU Delft, The Netherlands, with sp- sorship by the NIRICT Design Lab and Cadence Design Systems, and technical co-sponsorshipbytheIEEE.Furtherinformationabouttheworkshopisavailable athttp://ens.ewi.tudelft.nl/patmos09. The technical programof PATMOS 2009 contained state-of-the-arttechnical contributions, three invited keynotes, and a special session on SystemC-AMS Extensions. The technical program focused on timing, performance, and power consumption, as well as architectural aspects with particular emphasis on m- eling, design, characterization, analysis, and optimization in the nanometer era. The Technical Program Committee, with the assistance of additional expert reviewers, selected the 36 papers presented at PATMOS. The papers were - ganized into 7 oral sessions (with a total of 26 papers) and 2 poster sessions (with a total of 10 papers). As is customary for the PATMOS workshops, full papers were required for review, and a minimum of three reviews were received per manuscript.

Design for High Performance, Low Power, and Reliable 3D Integrated Circuits - Sung Kyu Lim 2012-11-27

This book provides readers with a variety of algorithms and software tools, dedicated to the physical design of through-silicon-via (TSV) based, three-dimensional integrated circuits. It describes numerous “manufacturing-ready” GDSII-level layouts of TSV-based 3D ICs developed with the tools covered in the book. This book will also feature sign-off level analysis of timing, power, signal integrity, and thermal analysis for 3D IC designs. Full details of the related algorithms will be provided so that the readers will be able not only to grasp the core mechanics of the physical design tools, but also to be able to reproduce and improve upon the results themselves. This book will also offer various design-for-manufacturability (DFM), design-for-reliability (DFR), and design-for-testability (DFT) techniques that are considered critical to the physical design process.

Design of High-performance, Low-power and Memory-efficient EBCOT and MQ Coder for JPEG2000 - 2003

High Performance Design Automation for Multi-Chip Modules and Packages -

Design and Modeling of Low Power VLSI Systems - Sharma, Manoj 2016-06-06

Very Large Scale Integration (VLSI) Systems refer to the latest development in computer microchips which are created by integrating hundreds of thousands of transistors into one chip. Emerging research in this area has the potential to uncover further applications for VSLI technologies in addition to system advancements. Design and Modeling of Low Power VLSI Systems analyzes various traditional and modern low power techniques for integrated circuit design in addition to the limiting factors of existing techniques and methods for optimization. Through a research-based discussion of the technicalities involved in the VLSI hardware development process cycle, this book is a useful resource for researchers, engineers, and graduate-level students in computer science and engineering.

Digital System Clocking - Vojin G. Oklobdzija 2005-03-11

Provides the only up-to-date source on the most recent advances inthis often complex and fascinating topic. The only book to be entirely devoted to clocking Clocking has become one of the most important topics in thefield of digital system design A "must have" book for advanced circuit engineers

Low-Power Electronics Design - Christian Piguet 2018-10-03

The power consumption of integrated circuits is one of the most problematic considerations affecting the design of high-performance chips and portable devices. The study of power-saving design methodologies now must also include subjects such as systems on chips, embedded software, and the future of microelectronics. Low-Power Electronics Design covers all major aspects of low-power design of ICs in deep submicron technologies and addresses emerging topics related to future design. This volume explores, in individual chapters written by expert authors, the many low-power techniques born during the past decade. It also discusses the many different domains and disciplines that impact power consumption, including processors, complex circuits, software, CAD tools, and energy sources and management. The authors delve into what many specialists predict about the future by presenting techniques that are promising but are not yet reality. They investigate nanotechnologies, optical circuits, ad hoc networks, e-textiles, as well as human powered sources of energy. Low-Power Electronics Design delivers a complete picture of today's methods for reducing power, and also illustrates the advances in chip design that may be commonplace 10 or 15 years from now.

Low Power Digital CMOS Design - Anantha P. Chandrakasan 2012-12-06

Power consumption has become a major design consideration for battery-operated, portable systems as well as high-performance, desktop systems. Strict limitations on power dissipation must be met by the designer while still meeting ever higher computational requirements. A comprehensive approach is thus required at all levels of system design, ranging from algorithms and architectures to the logic styles and the underlying technology. Potentially one of the most important techniques involves combining architecture optimization with voltage scaling, allowing a trade-off between silicon area and low-power operation. Architectural optimization enables supply voltages of the order of 1 V using standard CMOS technology. Several techniques can also be used to minimize the switched capacitance, including representation, optimizing signal correlations, minimizing spurious transitions, optimizing sequencing of operations, activity-driven power down, etc. The high- efficiency of DC-DC converter circuitry required for efficient, low-voltage and low-current level operation is described by Stratakos, Sullivan and Sanders. The application of various low-power techniques to a chip set for multimedia applications shows that orders-of-magnitude reduction in power consumption is possible. The book also features an analysis by Professor Meindl of the fundamental limits of power consumption achievable at all levels of the design hierarchy. Svensson, of ISI, describes emerging adiabatic switching techniques that can break the CV2f barrier and reduce the energy per computation at a fixed voltage. Srivastava, of AT&T, presents the application of aggressive shut-down techniques to microprocessor applications.

Soft Computing and Signal Processing - Jiacun Wang 2019-01-16

The book presents selected research papers on current developments in the field of soft computing and signal processing from the International Conference on Soft Computing and Signal Processing (ICSCSP 2018). It includes papers on current topics such as soft sets, rough sets, fuzzy logic, neural networks, genetic algorithms and machine learning, discussing various aspects of these topics, like technological, product implementation, contemporary research as well as application issues.

Oscillators and Oscillator Systems - Jan R. Westra 1999-10-31

In many electronic systems, such as telecommunication or measurement systems, oscillations play an essential role in the

information processing. Each electronic system poses different requirements on these oscillations, depending on the type and performance level of that specific system. It is the designer's challenge to find the specifications for the desired oscillation and to implement an electronic circuit meeting these specifications. As the desired oscillations have to fulfill many requirements, the design process can become very complex. To find an optimal solution, the designer requires a design methodology that is preferably completely top-down oriented. To achieve such a methodology, it must be assured that each property of the system can be optimized independently of all other properties. Oscillators and Oscillator Systems: Classification, Analysis and Synthesis takes a systematic approach to the design of high-performance oscillators and oscillator systems. A fundamental classification of oscillators, based on their internal timing references, forms the basis of this approach. The classification enables the designer to make strategic design decisions at a high hierarchical level of the design process. Techniques, derived from the systematic approach, are supplied to the designer to enable him or her to bring the performance of the system as close as possible to the fundamental limits. Oscillators and Oscillator Systems: Classification, Analysis and Synthesis is an excellent reference for researchers and circuit designers, and may be used as a text for advanced courses on the topic.

Transactions on High-Performance Embedded Architectures and Compilers II - Per Stenström 2009-04-22

This book contains extended versions of key papers from the 2nd International Conference on High-Performance Embedded Architectures and Compilers (HiPEAC 2007). It also covers such topics as microarchitecture, code generation, and performance modeling.

Power Aware Design Methodologies - Massoud Pedram 2007-05-08

Power Aware Design Methodologies was conceived as an effort to bring all aspects of power-aware design methodologies together in a single document. It covers several layers of the design hierarchy from technology, circuit logic, and architectural levels up to the system layer. It includes discussion of techniques and methodologies for improving the power efficiency of CMOS circuits (digital and analog), systems on chip, microelectronic systems, wirelessly networked systems of computational nodes and so on. In addition to providing an in-depth analysis of the sources of power dissipation in VLSI circuits and systems and the technology and design trends, this book provides a myriad of state-of-the-art approaches to power optimization and control. The different chapters of Power Aware Design Methodologies have been written by leading researchers and experts in their respective areas. Contributions are from both academia and industry. The contributors have reported the various technologies, methodologies, and techniques in such a way that they are understandable and useful.

Low-Power Low-Voltage Sigma-Delta Modulators in Nanometer CMOS - Libin Yao 2006-02-06

this book is not suitable for the bookstore catalogue

Die-stacking Architecture - Yuan Xie 2015-06-01

The emerging three-dimensional (3D) chip architectures, with their intrinsic capability of reducing the wire length, promise attractive solutions to reduce the delay of interconnects in future microprocessors. 3D memory stacking enables much higher memory bandwidth for future chip-multiprocessor design, mitigating the "memory wall" problem. In addition, heterogenous integration enabled by 3D technology can also result in innovative designs for future microprocessors. This book first provides a brief introduction to this emerging technology, and then presents a variety of approaches to designing future 3D microprocessor systems, by leveraging the benefits of low latency, high bandwidth, and heterogeneous integration capability which are offered by 3D technology.

Low Power Digital CMOS Design - Anantha P. Chandrakasan

1995-06-30

Power consumption has become a major design consideration for battery-operated, portable systems as well as high-performance, desktop systems. Strict limitations on power dissipation must be met by the designer while still meeting ever higher computational requirements. A comprehensive approach is thus required at all levels of system design, ranging from algorithms and architectures to the logic styles and the underlying technology. Potentially one of the most important techniques involves combining architecture optimization with voltage scaling, allowing a trade-off between silicon area and low-power operation. Architectural optimization enables supply voltages of the order of 1 V using standard CMOS technology. Several techniques can also be used to minimize the switched capacitance, including representation, optimizing signal correlations, minimizing spurious transitions, optimizing sequencing of operations, activity-driven power down, etc. The high- efficiency of DC-DC converter circuitry required for efficient, low-voltage and low-current level operation is described by Stratakos, Sullivan and Sanders. The application of various low-power techniques to a chip set for multimedia applications shows that orders-of-magnitude reduction in power consumption is possible. The book also features an analysis by Professor Meindl of the fundamental limits of power consumption achievable at all levels of the design hierarchy. Svensson, of ISI, describes emerging adiabatic switching techniques that can break the CV2f barrier and reduce the energy per computation at a fixed voltage. Srivastava, of AT&T, presents the application of aggressive shut-down techniques to microprocessor applications.

Coupled Data Communication Techniques for High-Performance and Low-Power Computing - Ron Ho 2010-06-03

Wafer-scale integration has long been the dream of system designers. Instead of chopping a wafer into a few hundred or a few thousand chips, one would just connect the circuits on the entire wafer. What an enormous capability wafer-scale integration would offer: all those millions of circuits connected by high-speed on-chip wires. Unfortunately, the best known optical systems can provide suitably ?ne resolution only over an area much smaller than a whole wafer. There is no known way to pattern a whole wafer with transistors and wires small enough for modern circuits. Statistical defects present a ?rmer barrier to wafer-scale integration. Flaws appear regularly in integrated circuits; the larger the circuit area, the more probable there is a ?aw. If such ?aws were the result only of dust one might reduce their numbers, but ?aws are also the inevitable result of small scale. Each feature on a modern integrated circuit is carved out by only a small number of photons in the lithographic process. Each transistor gets its electrical properties from only a small number of impurity atoms in its tiny area. Inevitably, the quantized nature of light and the atomic nature of matter produce statistical variations in both the number of photons de?ning each tiny shape and the number of atoms providing the electrical behavior of tiny transistors. No known way exists to eliminate such statistical variation, nor may any be possible.